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For Immediate Release

Cypress's *Warp*™ Leads Programmable Logic Into a New Era of HDL Design

Warp™ *Release 6.0 Suite Adds Functionality, Retains Industry-Leading Value Proposition; Targeted for Design of Delta39K™ Family of "CPLDs at FPGA Densities™"*

SAN JOSE, California…July 17, 2000 -- Cypress Semiconductor Corporation (NYSE:CY) today announced an upgrade of its popular *Warp*™ software design tools, introducing the *Warp* Release 6.0 family of programmable-logic design (PLD) software. Like previous versions of the *Warp* product, *Warp* Release 6.0 continues to provide a value-driven $99 edition along with two editions that provide additional design functionality.

Warp R6.0 retains and capitalizes on all the features and benefits of earlier *Warp* tool suites, which have helped Cypress become the No. 1 supplier of VHDL and Verilog-based PLD software with more than 25,000 installed seats. Cypress pioneered the use of HDL for programmable-logic design when it introduced *Warp* in 1991. Its leadership design tools accept design entry using VHDL IEEE-STD-1076/1164 or Verilog IEEE-STD-1364 and offer users the option to seamlessly integrate *Warp* software with all major third-party EDA environments. Because Cypress develops its own VHDL and Verilog synthesis software, its *Warp* tools provide the capabilities of tools costing much more, enabling designers to realize all of the performance and speed-to-market advantages of programmable logic without a large investment in software tools.

"Cypress has continually led the design tool revolution in this highly competitive business," said Christopher Norris, vice president of Cypress's Programmable Logic Division. “We were the first vendor to support VHDL, the first and only company to write its own HDL synthesis code, and the first to offer mass-market programmable-logic software with our high-quality, full-featured Warp2® for $99.00.

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"*Warp* Release 6.0 aims to build on our leadership position by continuing to provide high-value, high-quality design tools that support our new Delta39K™ CPLD family and all other Cypress programmable logic devices," Norris continued. "From a competitive standpoint, each of the three new *Warp* packages offer much more flexibility and functionality at a lower cost than any other tool available."

Architecture Explorer and Timing Analyzer

The Architecture Explorer and Timing Analyzer are new for Release 6.0, and were specifically engineered to allow designers to use Delta39K CPLDs more easily than FPGAs, even at high densities.

The Architecture Explorer provides design implementation analysis through graphical representation. Designers can zoom in to the macrocell level and view the equations for every signal. The Timing Analyzer allows designers to evaluate critical performance parameters by quickly reviewing the timing parameters for different signals. Designers then have the option to create specific sheets with user-defined timing parameters.

Designers can cross-probe between the Architecture Explorer and Timing Analyzer, using the architechture explorer to present a graphical view of paths highlighted in the Timing Analyzer. Using these tools, the numerical timing delays can be arranged and filtered in a variety of methods to explore asynchronous or synchronous paths within the design. Similar tools exist for FPGA devices, however since Delta39K is a CPLD, the Architecture Explorer and Timing Analyzer present design equations as they were implemented in the device – in Sum-of-Products form. This is the first time in PLD history that 100K+ gate designs can be debugged as easily as 22V10 designs once were – by examining the design equations graphically at each macrocell.

Many of the new features in *Warp* Release 6.0 are based on Active-HDL™ from Aldec Inc. Cypress includes Aldec's Graphical Finite State Machine Editor and Timing Analyzer in its $99 *Warp* software. *Warp* Professional and Enterprise products also provide additional, high-end Aldec tools, such as a graphical HDL block editor, automatic text HDL to graphical design translation, HDL source code debugging, and full behavioral and timing simulation with testbench support.

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***Warp* R6.0 Editions**

Under *Warp* R6.0, Cypress will offer three new *Warp* products at different price and value points:

	***Warp*™**	***Warp*™ Professional**	***Warp*™ Enterprise**
Price	$99	$495	$2995
Timing Analyzer	√	√	√
Architecture Explorer	√	√	√
VHDL/Verilog synthesis	√	√	√
FSM editor	√	√	√
Supports Cypress CPLDs	√	√	√
HDL text editor	√	√	√
Block diagram editor		√	√
Waveform comparison		√	√
Language assistant		√	√
Auto HDL to graphics			√
Functional simulation			√
Testbench generation			√

"For $99, *Warp*'s flexible simulation options allow you to debug your design's functionality and verify your timing with industry-standard, IEEE-compliant VHDL and Verilog simulation models--using the Cypress simulator included or any other HDL simulator on the market," Norris said. "With *Warp*, you get the best HDL solution available from a single, cost-effective, high-quality tool that is easy to use and supports all of Cypress's programmable-logic devices."

Cypress's Warp R6.0 can be used as a standalone CPLD development system or seamlessly integrated with third-party EDA environments. Cypress CPLD devices are supported by third-party synthesis tools from Aldec, Cadence, Exemplar Logic, Innoveda, Mentor Graphics, Synopsys, Synplicity, and more. Every *Warp* suite can operate over all major operating systems, including Windows 95/98, Windows NT, Sun Solaris, and HP workstations. This broad support allows virtually all designers to design with Cypress programmable logic offerings.

Free Upgrades

As it has since *Warp*'s introduction, Cypress continues to provide existing users of its *Warp* products free registration and upgrades to *Warp* R6.0 for life. Users simply need to register with Cypress to continue receiving upgrades.

For new users, *Warp* R6.0 is available now for $99 via download from Cypress's web site at http://www.cypress.com/pld/warp.html. *Warp* R6.0, Professional and Enterprise will be available on CD-ROM August 14, 2000. Customers can call Cypress's toll free hotline at (800) *WARP*-VHDL (927-7843), and order the software using a Visa or Mastercard. For more information, customers can call (800) 858-1810 in North America or (408) 943-2600.

About Cypress

Cypress Semiconductor provides high-performance integrated circuit solutions "By Engineers. For Engineers.™" for fast-growing companies in fast-growing markets, including data communications, telecommunications, computation, consumer products, and industrial-control. With a focus on emerging communications applications, Cypress's product lines include networking-optimized and micropower static RAMs; high-bandwidth multiport and FIFO memories; high-density programmable logic devices; timing technology for PCs and other digital systems; and controllers for Universal Serial Bus (USB). Cypress is No. 1 in the USB and clock chip markets.

Cypress employs more than 3,900 people worldwide with international headquarters in San Jose, California. Its shares are listed on the New York Stock Exchange under the symbol CY. More information about Cypress is accessible electronically on the company's worldwide web site at http://www.cypress.com or by CD-ROM (call 1-800-858-1810). An electronic investor forum, and other investor information, is located at http://www.cypress.com/investor/index.html.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements herein that are not historical facts are "forward-looking statements" involving risks and uncertainties. Please refer to Cypress's Securities and Exchange Commission filings for a discussion of such risks.

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